UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/537,274	03/29/2000	Larry Eugene Mosley	884.240US1	7167

21186 7590 04/16/2003

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER
THOMAS, ERIC W

ART UNIT	PAPER NUMBER
2831	15

DATE MAILED: 04/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/537,274	MOSLEY, LARRY EUGENE	
	Examiner	Art Unit	
	Eric W Thomas	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-7 and 9-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6,7 and 9-18* is/are allowed.

6)☒ Claim(s) *2-5,19 and 21* is/are rejected.

7)☐ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *20 August 2001* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Introduction:

The examiner acknowledges, as recommended in the M.P.E.P., the applicant's submission of the amendment dated 1/21/03. At this point claims 2, 4, 6, and 7 have been amended; and claims 1 and 8 have been cancelled. Claims 2-7, 9-21 are pending in the instant application.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

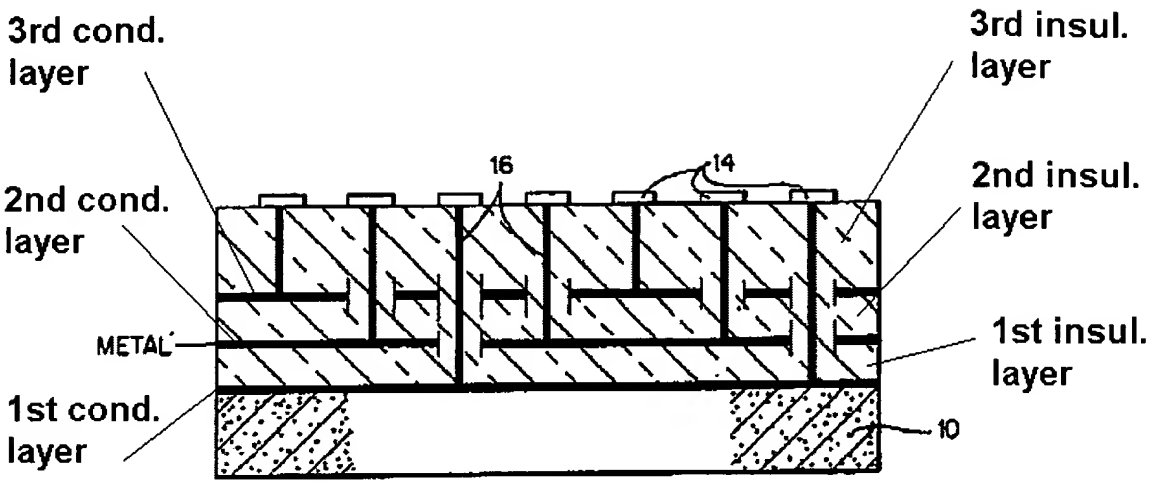
Claim 21 depends on a cancelled claim. The examiner examined this claim as if it depended on claim 2.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4-5, 19, are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM Technical disclosure bulletin (Cross-reference 0018-8689-20-8-3117 – Referred as '3117).



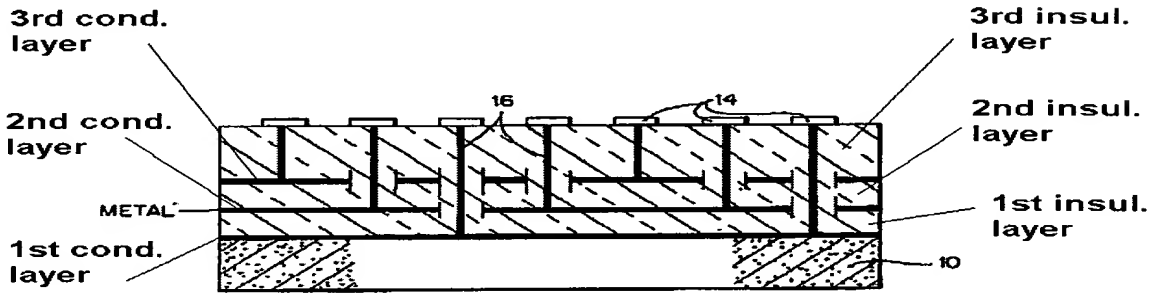
'3117 discloses a multi layer integrated circuit capacitor comprising: a substrate (10); a first conductive layer located over and contacting the substrate (see above);

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate; a second conductive layer located over the first insulator layer; a second insulator layer located over the second conductive layer; a third conductive layer located over the second insulator layer; a third insulator layer located over the third conductor layer; and a plurality of conductive vias (16) downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers.

'3117 discloses the claimed invention except for the insulator layers are formed from a BaSrTiO3 material. It is well known in the capacitor art to form insulating layers from a BaSrTiO3 material (excellent dielectric properties). It

would have been obvious to one having ordinary skill in the art at the time the invention was made to form the dielectric from a BaSrTiO3, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claim 5, '3117 discloses the claimed invention for the conductive layers are formed from copper. It is well know in the capacitor art to form conductive layers (electrodes) from a copper material (excellent conductive properties). It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the conductive layers from a copper material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

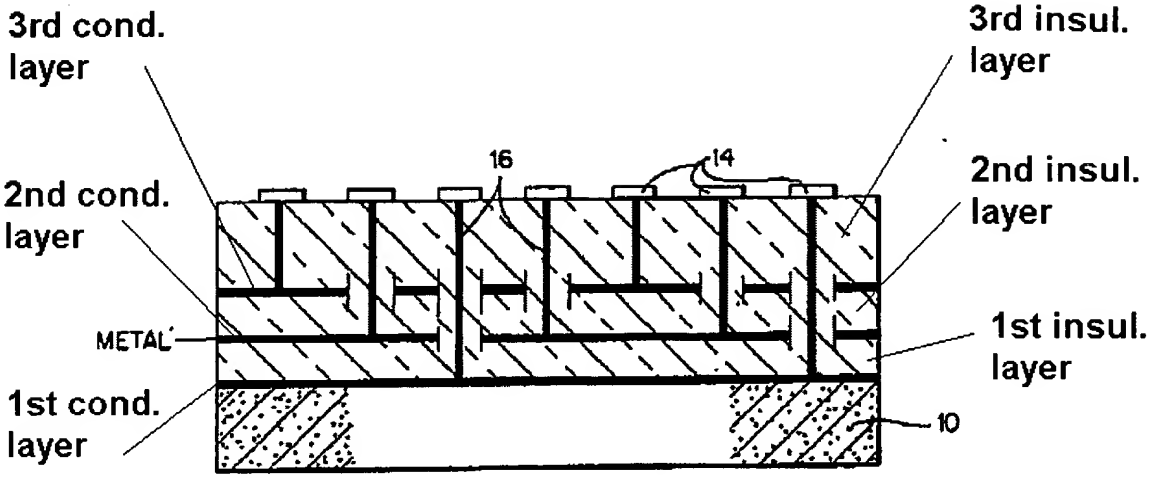


Regarding claim 19, '3117 discloses a multi layer integrated circuit capacitor comprising: a substrate (10); a first conductive layer located over and contacting the substrate (see above); a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate; a second conductive layer located over the first insulator layer; a

second insulator layer located over the second conductive layer; a third conductive layer located over the second insulator layer; a third insulator layer located over the third conductor layer; and a plurality of conductive vias (16) downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers.

'3117 discloses the claimed invention except for the plurality of vias extending through the substrate to provide electrical interconnection to both a top surface and a bottom surface of the integrated circuit capacitor. It is well known in the capacitor art to extend vias through a substrate to provide electrical interconnections to both sides of the capacitive element. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to extend the vias of '3117 through the substrate to provide electrical interconnections to both sides of the capacitor, since such a modification would decrease the space needed in the electrical system.

3. Claims 2-3, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM Technical disclosure bulletin (Cross-reference 0018-8689-20-8-3117 – Referred as '3117) in view of Herrell (US 6,191,479).



'3117 discloses a multi layer integrated circuit capacitor comprising: a substrate (10); a first conductive layer located over and contacting the substrate (see above);

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate; a second conductive layer located over the first insulator layer; a second insulator layer located over the second conductive layer; a third conductive layer located over the second insulator layer; a third insulator layer located over the third conductor layer; and a plurality of conductive vias (16) downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers.

'3117 disclose the claimed invention except for a plurality of controlled collapse chip connection (C4) lands fabricated on and contacting the third insulator layer and in electrical contact with the plurality of conductive vias. '3117

illustrates voltage supply pads formed on and contacting the third insulator layer and in electrical contact with the plurality of conductive vias. The capacitor is connected to a chip by short metal lines (see fig. 2).

Herrell teaches the use of C4 lands that electrically contacts vias in the capacitor art. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the capacitor of '3117 using the C4 lands as taught by Herrell, since such a modification would decrease the space used in the electrical system by placing the capacitor directly onto the chip.

Regarding claim 3, '3117 disclose the claimed invention except for C4 lands fabricated in staggered columns in a plan view. '3117 illustrates a column of voltage supply pads arranged on a capacitor. Herrell illustrates multiple C4 lands fabricated in staggered columns in a plan view. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form multiple C4 lands which is fabricated in staggered columns in a plan view, since such a modification would allow additional connections to the capacitor of '3117.

Regarding claim 21, '3117 discloses the claimed invention for the conductive layers are formed from copper. It is well know in the capacitor art to form conductive layers (electrodes) from a copper material (excellent conductive properties). It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the conductive layers from a copper material, since it has been held to be within the general skill of a worker in the art

to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

'3117 discloses the claimed invention except for the insulator layers are formed from a BaSrTiO3 material. It is well known in the capacitor art to form insulating layers from a BaSrTiO3 material (excellent dielectric properties). It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the dielectric from a BaSrTiO3, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Allowable Subject Matter

4. Claims 6-7, 9-18 are allowed.

5. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments, see page 4, filed 1/21/03, with respect to claims 11 and 13 have been fully considered and are persuasive. The rejection of claims 11 and 13 has been withdrawn.

Official Notice

A) "Applicant objects to the official notice (with regard to the materials used for the insulator and electrode) using a single reference and respectfully

request that additional references be cited in support of this position." The examiner addressed this objection in the final action dated 11/7/01 (see below).

Strontium Barium Titanate (SBT) is a well-known dielectric material used in the capacitor art. SBT is known for its high dielectric constant. See US 5,679,980; 5,793,057; 5,811,851; 5,781,404; 5,729,054; & 5,696,018.

Copper is a well-known electrode material. Copper has excellent electro-conductivity. See 5,910,881; 5,471,363; 5,512,353 5,093,757; 5,159,524; 5,117,326; 5,107,394; & 6,101,693.

B) "Applicant objects to the official notice (with regard to the vias extending through the substrate to provide electrical interconnects on the bottom side of the capacitor) using a single reference and respectfully request that additional references be cited in support of this position."

Fig. 6 of Kuroda et al. (US 6,351,369 and 6,370,010) illustrate vias that extend through a substrate to provide interconnects to the capacitor.

'3117 in view of Herrell

7. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.**

See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric W Thomas whose telephone number is (703) 305-0878. The examiner can normally be reached on Mon & Sat 9:00AM - 9:30PM; Tues-Fri 5:30PM-10:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 703-308-3682. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Dean A. Reichard 4/15/03

DEAN A. REICHARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800